ABSTRACT OF THE DISCLOSURE

A semiconductor storage device which can be evaluated correctly. A shift processing circuit 5 sequentially shifts row addresses in a line direction to reassign them in a memory cell array MSA10. A data inversion determination unit 8 identifies bit line pairs BL1, ..., BL128 of which the wire position switching parts CCAR10 and CCAR11 cross a word line specified by an input row address, according to the twisting positions and shift, to determines whether to invert the level of evaluation test data D8 which is input/output to/from the bit line pairs BL1, ..., BL128. The inversion processor 4 inverts the level of the evaluation test data D8 which is input to and output from the bit line pairs BL1, ..., BL128, to correctly store the evaluation test data D8 of level "0", "1" in memory cells in a storing pattern and output the data by offsetting the inversion applied at the time of storage. As a result, the semiconductor storage device can be evaluated correctly.